REMARKS/ARGUMENTS

Applicant received the Office Action dated June 11, 2008 in which the Examiner: 1) rejected claims 1–7 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. App. Pub. No. US 2004/0174831 ("*Yi*") in view of U.S. Patent No. 6,182,202 ("*Muthukkaruppan*") and 2) rejected claims 11, 12 and 19-21 under 35 U.S.C. § 103(a) as being unpatentable over *Yi* in view of *Muthukkaruppan* and U.S. Pat. App. Pub. No. US 2004/0002366 ("*Cromer*"). The Examiner also appears to reject claims 8 and 10 in view of *Yi* and *Muthukkaruppan* and to reject claims 13-17 in view of *Yi*, *Muthukkaruppan* and *Cromer*.

Based on the arguments contained herein, Applicant respectfully requests reconsideration and allowance of the pending claims.

§ 103 REJECTIONS

The Examiner rejected claims 1-8 and 10 as being unpatentable over *Yi* in view of *Muthukkaruppan*. Any rejection under 35 U.S.C. § 103 must clearly and explicitly articulate the reason(s) why the claimed invention would have been obvious. MPEP § 2142. The framework for determining obviousness under 35 U.S.C. § 103 requires (1) determination of the scope and content of the prior art; (2) assessment of the differences between the claimed invention and the prior art; and (3) assessment of the level of ordinary skill in the pertinent art. *MPEP* § 2141 (citing *KSR International Co. v. Teleflex Inc.*, 127 S. Ct. 1727 (2007)). Differences between the claim limitations and the prior art weighs in favor of non-obviousness. To establish obviousness, each of the claim limitations must be taught or suggested by the prior art. See *CFMT, Inc. v. YieldUp Int'l Corp.*, 349 F.3d 1333, 1342 (Fed. Cir. 2003). The Examiner's rejection of claims 1-8 and 10 is improper for the reasons set forth below.

Claim 1, in part, requires "the slave device is configurable by the master device to operate in multiple modes including a direct memory addressing mode and an indirect memory addressing mode" and "fewer bits are serially transferred between the master device and the slave device for reads and writes in the indirect memory addressing mode

than for reads and writes in the direct memory addressing mode." The Examiner concedes that *Yi* does not teach or suggest direct and indirect memory addressing modes as in claim 1, but cites *Muthukkaruppan* as teaching these modes. See Office Action dated 06/11/08, page 3, first full paragraph. *Muthukkaruppan* mentions direct and indirect addressing modes, but does not teach or suggest a slave device being configured by a master device to operate in such modes as in claim 1. On the contrary, *Muthukkaruppan* only shows a single device (computer 200) that implements direct or indirect addressing modes based on control codes 310, 318 and 324. *Muthukkaruppan* does not describe the computer 200 as a slave device and the control codes appear to be generated by the computer 200 itself rather than another device.

Furthermore, *Muthukkaruppan* applies the variable operand offset technique for both direct and indirect addressing modes (see e.g., col 4, lines 32-35 and col. 7, line 57 – col. 8, line 3). Because *Muthukkaruppan*'s technique of using variable operand offsets to reduce wasted memory space and processing applies to both direct and indirect addressing modes, *Muthukkaruppan* does not actually teach that indirect memory addressing involves fewer bits than direct memory addressing as in claim 1. *Muthukkaruppan* simply describes indirect memory addressing by stating "in an indirect addressing mode, the address specified in the computer instruction is an address at which is stored an address that specifies the memory location that contains the data that is to be used for the operand" (col. 1, lines 28-32) and thus does not require that indirect memory addressing have fewer bits than direct memory addressing.

The Examiner appears to recognize *Muthukkaruppan's* deficiencies and mentions paragraphs [0002]-[0006] of U.S. Pat. App. Pub. No. 2004/0054949 ("*Hunt*") to support the argument that indirect addressing obviously uses fewer bits than direct addressing. See Office Action dated 06/11/08, page 4, first paragraph. However, *Hunt* implements a multi-bit bus (e.g., a 32-bit bus) for parallel communications rather than a serial communication interface as in claim 1. Further, *Hunt* does not teach that indirect addressing uses fewer total bits than direct addressing as is suggested by the Examiner. Instead, *Hunt* teaches that indirect addressing occupies a smaller address space on the

bus (paragraph [0006]), but requires two direct address transactions (see paragraphs [0007]-[0008]). Thus, the total number of bits needed for indirect addressing in *Hunt* (two sequential transactions) could actually be more than the total number of bits required for direct addressing. At any rate, such bits are not serially transferred as in claim 1. The Examiner has not clarified these issues and thus has failed to clearly and explicitly articulate the reasons why the claimed invention would have been obvious as is required. For at least these reasons, claim 1 and its dependent claims are allowable over *Yi* and *Muthukkaruppan*.

Claim 8, in part, requires "the processor and the slave device are configurable to communicate in multiple modes, each mode being associated with a different read/write command length." The Examiner argues that *Muthukkaruppan's* direct/indirect address modes teach Applicants' claimed "multiple modes" limitation. See Office Action dated 06/11/08, page 4, last paragraph. As previously discussed with respect to claim 1, *Muthukkaruppan* teaches that variable operand offsets can be used for both direct and indirect addressing modes. Because *Muthukkaruppan's* Fig. 3 is described as being applicable to both direct and indirect addressing modes (see e.g., col. 7, lines 57-60), it appears that both modes use the same command length (12 bytes) rather than different command lengths as in claim 8. Further, the other variable operand offset schemes described in *Muthukkaruppan* (e.g., Figs. 4-6) are not described as varying depending on whether a direct and indirect addressing mode is used. The Examiner has not clarified these issues and thus has failed to clearly and explicitly articulate the reasons why the claimed invention would have been obvious as is required. For at least these reasons, claim 8 and its dependent claims are allowable over *Yi* and *Muthukkaruppan*.

Claim 13 was rejected as being unpatentable over *Yi* in view of *Muthukkaruppan* and *Cromer*. Claim 13, in part, requires "configuring the device to interpret read/write commands having a reduced length if the power consumption parameter exists." The Examiner appears to concede that *Yi* and *Muthukkaruppan* do not teach the above limitation, but relies on *Cromer* as teaching this limitation. See Office Action dated 06/11/08, page 6, second full paragraph. As already discussed in previous responses,

the Examiner is misapplying *Cromer*. In *Cromer*, the speed of data transmission (the frequency of symbol transmission) is adjusted (see Fig. 2 and paragraph [0014]), but not the total number of bits being transmitted. The frequency of symbol transmission in *Cromer* has nothing to do with read/write commands having a reduced length (*i.e.,* a reduced number of data bits) as in claim 13. None of the cited references, considered individually or together, teaches or suggests the above limitation. For at least these reasons, claim 13 and its dependent claims are allowable over *Yi*, *Muthukkaruppan* and *Cromer*.

Claim 19, in part, requires "means for configuring the second device in a first mode associated with read/write commands having a non-reduced address field" and "means for configuring the second device in a second mode associated with read/write commands having a reduced address field." Claim 19 further requires "means for conveying a "not busy" signal from the slave device to the master device during the first and second modes, the "not busy" signal having fewer bits in the second mode than in the first mode."

For much the same reasons as given for claim 1, *Muthukkaruppan* does not teach or suggest the claimed "first mode" and "second mode". Again, *Muthukkaruppan's* variable operand offsets can be used for both direct and indirect addressing modes. In other words, *Muthukkaruppan* teaches reduced operand offset fields for both direct and indirect memory addressing rather than a first mode having a non-reduced address field and a second mode having a reduced address field as in claim 19.

Further, *Yi* does not teach or suggest a "not busy" signal "having fewer bits in the second mode than in the first mode" as in claim 19. The Examiner cites paragraph [0011] of *Yi* as teaching this limitation. See Office Action dated 06/11/08, page 6, last paragraph. However, Applicants cannot find where *Yi* teaches a "not busy" signal and much less one "having fewer bits in the second mode than in the first mode" as in claim 19. Paragraph [0011] of *Yi* simply describes data transmission between a master and slave without addressing Applicants' claimed "not busy" signal. Thus, the Examiner has failed to clearly and explicitly articulate the reasons why the claimed invention would have

been obvious as is required. *Cromer* does not overcome the deficiencies of *Muthukkaruppan* and *Yi* with regard to the above limitations. For at least these reasons, claim 19 and its dependent claims are allowable over *Yi* and *Muthukkaruppan*.

CONCLUSION

In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

Applicant respectfully requests reconsideration and that a timely Notice of Allowance be issued in this case. Applicant hereby petitions for any time extensions that are necessary to prevent this case from being abandoned. In the event that additional fees related to this Amendment, or other transactions in this case, are required (including fees for net addition of claims and for time extension), the Examiner is authorized to charge Texas Instruments Incorporated's Deposit Account No. 20-0668 for such fees.

Respectfully submitted,

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